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Section 2

Molecular and Nano-Electronics: Concepts, Challenges, and Designs

3

Engineering Challenges in Molecular Electronics

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Abstract

This article discusses molecular electronics in the context of silicon materials and device engineering. Historic trends in silicon devices — and engineering scaling rules that dictate these trends — give insight into how silicon has become so dominant an electronic material and how difficult it will be to challenge silicon devices with a distinctly different *leapfrog* technology. Molecular electronics presents some intriguing opportunities, and it is likely that these opportunities will be achieved through hybrid silicon/molecular devices that incorporate beneficial aspects of both material systems.

3.1 Introduction

Manufacturing practices for complementary metal oxide semiconductor (CMOS) devices are arguably the most demanding, well developed, and lucrative in history. Even so, it is well recognized that historic trends in device scaling that have continued since the 1960s are going to face serious challenges in the next several years. Current trends in Moore's Law scaling are elucidated in detail in the Semiconductor

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Industry Association's *The International Technology Roadmap for Semiconductors*.[1] The 2001 roadmap highlights significant fundamental barriers in patterning, front-end processes, device structure and design, test equipment, interconnect technology, integration, assembly and packaging, etc.; and there are significant industry and academia research efforts focused on these challenges. There is also significant growing interest in potential leapfrog technologies, including quantum-based structures and molecular electronics, as possible means to redefine electronic device and system operation. The attention (and research funds) applied to potential revolutionary technologies is small compared with industrial efforts on silicon. This is primarily because of the tremendous manufacturing infrastructure built for silicon technology and the fact that there is still significant room for device performance improvements in silicon — even though many of the challenges described in the roadmap still have "no known solution." Through continued research in leapfrog approaches, new materials and techniques are being developed that could significantly impact electronic device manufacturing. However, such transitions are not likely to be realized in manufacturing without improved insight into the engineering of current high-performance electronic devices.

Silicon devices are highly organized inorganic structures designed for electronic charge and energy transduction.[2–4] Organic molecules are also highly organized structures that have well-defined electronic states and distinct (although not yet well-defined) electronic interactions within and among themselves. The potential for extremely high device density and simplified device fabrication has attracted attention to the possibility of using individual molecules for advanced electronic devices (see recent articles by Ratner;[5] Kwok and Ellenbogen;[6] and Wada[7]). A goal of molecular electronics is to use fundamental molecular-scale electronic behavior to achieve electronic systems (with functional logic and/or memory) composed of individual molecular devices. As the field of molecular electronics progresses, it is important to recognize that current silicon circuits are likely the most highly engineered systems in history, and insight into the engineering driving forces in silicon technology is critical if one wishes to build devices more advanced than silicon. The purpose of this article, therefore, is to give a brief overview of current semiconductor device operation, including discussion of the strengths and weaknesses of current devices and, within the context of current silicon device engineering, to present and discuss possible routes for molecular electronics to make an impact on advanced electronics engineering and technology.

3.2 Silicon-Based Electrical Devices and Logic Circuits

3.2.1 Two-Terminal Diode and Negative Differential Resistance Devices

The most simple silicon-based solid-state electronic device is the p/n junction diode, where the current through the two terminals is small in the reverse direction and depends exponentially on the applied voltage in the forward direction. Such devices have wide-ranging applications as rectifiers and can be used to fabricate memory and simple logic gates.[8,9] A variation on the p/n diode is a resonant tunneling diode (RTD) where well-defined quantum states give rise to negative differential resistance (NDR). A schematic current vs. voltage trace for an NDR device is shown in Figure 3.1. Such devices can be made with inorganic semiconductor materials and have been integrated with silicon transistors[10–13] for logic devices with multiple output states to enhance computation complexity.

An example circuit for an NDR device with a load resistor is shown in Figure 3.1. This circuit can act as a switch, where V_{out} is determined by the relative voltage drop across the resistor and the diode. The resistance of the diode is switched from high to low by applying a short voltage pulse in excess of V_{dd} across the series resistor and diode, and the smaller resistance results in a small V_{out}. These switching circuits may be useful for molecular logic gates using RTD molecules, but several important issues need to be considered for applications involving two-terminal logic. One concern is the size of the output impedance. If the outlet voltage node is connected to a resistance that is too small (i.e., similar in magnitude to the RTD impedance), then the outlet voltage (and voltage across the RTD) will shift from the expected value; and this error will propagate through the circuit network. Another concern is that full logic gates fabricated with RTDs require an additional clock signal, derived from a controlled oscillator

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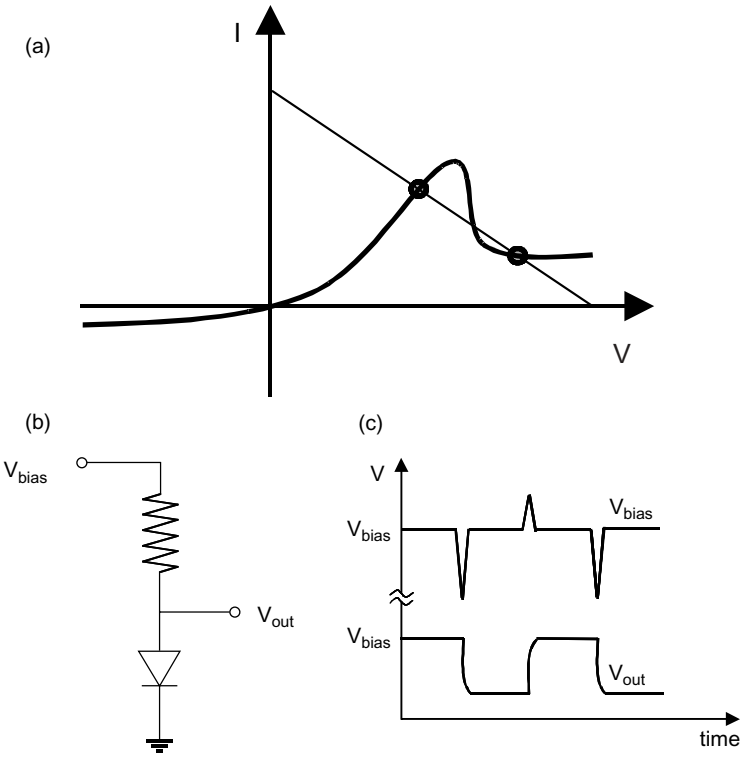

FIGURE 3.1 Schematic of one possible NDR device. (a) Schematic current vs. voltage curve for a generic resonant tunneling diode (RTD) showing negative differential resistance (NDR). The straight line is the resistance load line, and the two points correspond to the two stable operating points of the circuit. (b) A simple circuit showing an RTD loaded with a resistor. (c) Switching behavior of resistor/RTD circuit. A decrease in V_{bias} leads to switching of the RTD device from high to low impedance, resulting in a change in V_{out} from high to low state.

circuit. Such oscillators are readily fabricated using switching devices with gain, but to date they have not been demonstrated with molecular devices. Possibly the most serious concern is the issue of power dissipation. During operation, the current flows continuously through the RTD device, producing significant amounts of thermal energy that must be dissipated. As discussed below in detail, power dissipation in integrated circuits is a long-standing problem in silicon technology, and methodologies to limit power in molecular circuits will be a critical concern for advanced high-density devices.

3.2.2 Three-Terminal Bipolar, MOS, and CMOS Devices

The earliest solid-state electronic switches were bipolar transistors, which in their most simple form consisted of two back-to-back p/n junctions. The devices were essentially solid-state analogs of vacuum tube devices, where a current on a base (or grid) electrode modulated the current between the emitter and collector contacts. Because a small change in the base voltage, for example, could enable a large change in the collector current, the transistor enabled signal amplification (similar to a vacuum tube device) and, therefore, current or voltage gain. In the 1970s, to reduce manufacturing costs and increase integration capability, industry moved away from bipolar and toward metal-oxide-semiconductor field effect transistor (MOSFET) structures, shown schematically in Figure 3.2. For MOSFET device operation, voltage applied to the gate electrode produces an electric field in the semiconductor, attracting charge to the silicon/dielectric interface. A separate voltage applied between the source and drain then enables current to flow to the drain in a direction perpendicular to the applied gate field. Device geometry is determined by the need for the field in the channel to be determined primarily by the gate voltage and

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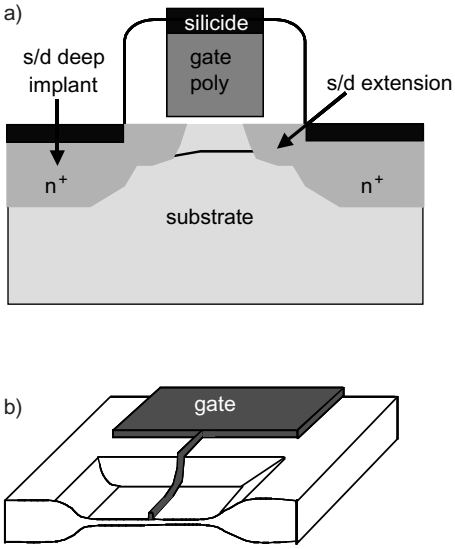

FIGURE 3.2 (a) Cross section of a conventional MOS transistor. (b) A three-dimensional representation of a MOS transistor layout. Two transistors, one NMOS and one PMOS, can be combined to form a complementary MOS (CMOS) device.

not by the voltage between the source and drain. In this structure, current flow to or from the gate electrode is limited by leakage through the gate dielectric. MOS devices can be either NMOS or PMOS, depending on the channel doping type (p- or n-type, respectively) and the charge type (electrons or holes, respectively) flowing in the inversion layer channel. Pairing of individual NMOS and PMOS transistors results in a complementary MOS (CMOS) circuit.

3.2.3 Basic Three-Terminal Logic Circuits

A basic building block of MOS logic circuits is the signal inverter, shown schematically in Figure 3.3. Logic elements, including, for example, NOR and NAND gates, can be constructed using inverters with multiple inputs in parallel or in series. Early MOS circuits utilized single-transistor elements to perform the inversion function utilizing a load resistor as shown in Figure 3.3a. In this case, when the NMOS is off (V_{in} is less than the device threshold voltage V_{th}), the supply voltage (V_{dd}) is measured at the outlet. When V_{in} is increased above V_{th}, the NMOS turns on and V_{dd} is now dropped across the load resistor; V_{out} is now in common with ground, and the signal at V_{out} is inverted relative to V_{in}. The same behavior is observed in enhancement/depletion mode circuits (Figure 3.3b) where the load resistor is replaced with another NMOS device. During operation of these NMOS circuits, current is maintained between V_{dd} and ground in either the high- or low-output state. CMOS circuits, on the other hand, involve combinations of NMOS and PMOS devices and result in significantly reduced power consumption as compared with NMOS-only circuits. This can be seen by examining a CMOS inverter structure as shown in Figure 3.3c. A positive input voltage turns on the NMOS device, allowing charge to flow from the output capacitance load to ground and producing a low V_{out}. A low-input voltage likewise enables the PMOS to turn on, and the output to go to the level of the supply voltage, V_{dd}. During switching, current is required to charge and discharge the channel capacitances, but current stops flowing when the channel and output capacitances are fully charged or discharged (i.e., when V_{out} reaches 0 or V_{dd}). In this way, during its static state, one of the two transistors is always off, blocking current from V_{dd} to ground. This means that the majority of the power consumed in an array of these devices is determined by the rate of switching and not by the number of inverters in the high- or low-output state within the array. This is a tremendously important outcome of the transition in silicon technology from NMOS to CMOS: *the*

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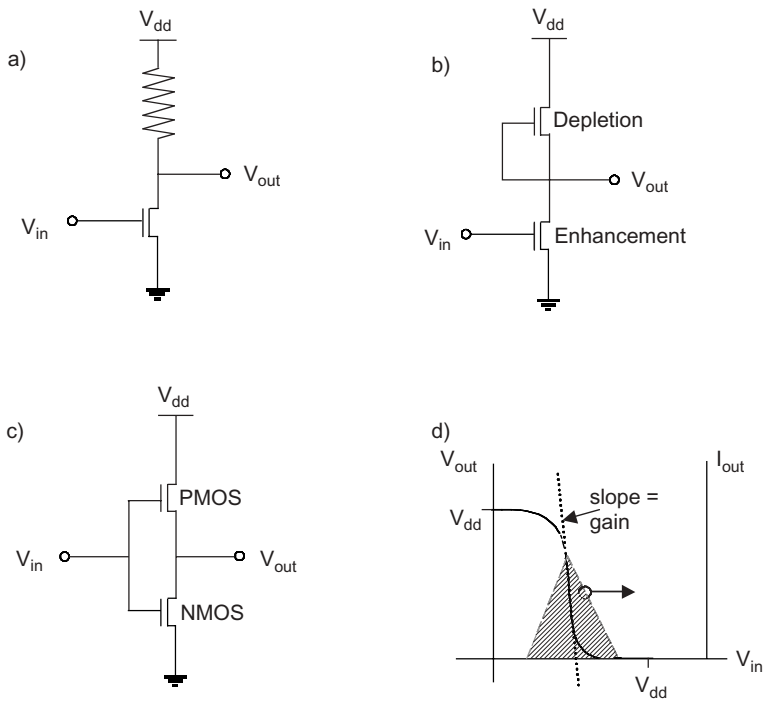

FIGURE 3.3 Inverter circuit approaches for NMOS and CMOS devices. (a) A simple inverter formed using an NMOS device and a load resistor, commonly used in the 1970s. (b) An inverter formed using an NMOS device and a depletion-mode load transistor. (c) Complementary MOS (CMOS) inverter using an NMOS and a PMOS transistor, commonly used since the 1980s. (d) A schematic voltage inverter trace for a CMOS inverter. The slope of the V_{out} vs. V_{in} gives the inverter gain. Also shown is the net current through the device as a function of V_{in}. Note that for the CMOS structure, current flows through the inverter only during the switching cycle, and no current flows during steady-state operation.

power produced per unit area of a CMOS chip can be maintained nearly constant as the number density of individual devices on the chip increases. The implications for this in terms of realistic engineered molecular electronic systems will be discussed in more detail below.

3.2.4 The Importance of Gain

Gain in an electronic circuit is generally defined as the ratio of output voltage change to input voltage change (i.e., voltage gain) or ratio of output current change to input current change (current gain). For a simple inverter circuit, therefore, the voltage gain is the slope of the V_{out} vs. V_{in} curve, and the maximum gain corresponds to the value of the maximum slope. A voltage gain in excess of one indicates that if a small-amplitude voltage oscillation is placed on the input (with an appropriate dc bias), a larger oscillating voltage (of opposite phase) will be produced at the output. Typical silicon devices produce gain values of several hundred. Power and voltage gain are the fundamental principles behind amplifier circuits used in common electronic systems, such as radios and telephones.

Gain is also critically important in any electronic device (such as a microprocessor) where voltage or current signals propagate through a circuit. Without gain, the total output power of any circuit element will necessarily be less than the input; the signal would be attenuated as it moved through the circuit, and eventually *high* and *low* states could not be differentiated. Because circuit elements in silicon technology produce gain, the output signal from any element is "boosted" back up to its original input value; and the signal can progress without attenuation.

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In any system, if the power at the output is to be greater than the power at an input reference, then an additional input signal will be required. Therefore, at least three contact terminals are required to achieve gain in any electronic element: high voltage (or current) input, small voltage or current input, and large signal output. The goal of demonstrating molecular structures with three terminals that produce gain continues to be an important challenge.

3.3 CMOS Device Parameters and Scaling

3.3.1 Mobility and Subthreshold Slope

The speed of a circuit is determined by how fast a circuit output node is charged up to its final state. This is determined by the transistor drive current, which is related to the device dimension and the effective charge mobility, μ_{eff} (or transconductance), where mobility is defined as charge velocity per unit field. In a transistor operating under sufficiently low voltages, the velocity will increase in proportion to the lateral field (V_{sd}/L_{ch}), where V_{sd} is the source/drain voltage and L_{ch} is the effective length of the channel. At higher voltages, the velocity will saturate, and the lateral field becomes nonuniform. This *saturation velocity* is generally avoided in CMOS circuits but becomes more problematic for very short device lengths. Saturation velocity for electrons in silicon at room temperature is near 10^7cm/s, and it is slightly smaller for holes. For a transistor operating with low voltages (i.e., in the linear regime), the mobility is a function of the gate and source/drain voltages (V_{gs} and V_{sd}), the channel length and width (L_{ch} and W_{ch}) and the gate capacitance per unit area (C_{ox}; Farads/cm^2):

$$\mu_{eff} = \frac{I_{sd}L_{ch}}{C_{ox}W_{ch}(V_{gs} - V_{th})V_{sd}} \tag{3.1}$$

The mobility parameter is independent of device geometry and is related to the current through the device. Because the current determines the rate at which logic signals can move through the circuit, the effective mobility is an important figure of merit for any electronic device.

Another important consideration in device performance is the subthreshold slope, defined as the inverse slope of the log (I_{sd}) vs. V_g curve for voltages below V_{th}. A typical current vs. voltage curve for an NMOS device is shown in Figure 3.4. In the subthreshold region, the current flow is exponentially dependent on voltage:

$$I_{sd} \propto \exp(qV/nkT) \tag{3.2}$$

where n is a number typically greater than 1. At room temperature, the ideal case (i.e., minimal charge scattering and interface charge trapping) results in n = 1 and an inverse slope $(2.3 \cdot kT)/q \approx 60$mV/decade. The subthreshold slope of a MOS device is a measure of the rate at which charge diffuses from the channel region when the device turns off. Because the rate of charge diffusion does not change with device dimension, the subthreshold slope will not change appreciably as transistor size decreases. The nonscaling of subthreshold slope has significant implications for device scaling limitations. Specifically, it puts a limit on how much V_{th} can be reduced because the current at zero volts must be maintained low to control off-state current, I_{off}. This in turn puts a limit on how much the gate voltage can be decreased, which means that the ideal desired constant field scaling laws, described below, cannot be precisely followed.

Neither the mobility nor subthreshold slope is significantly affected by reduction in transistor size. Under ideal constant field scaling, the channel width, length, and thickness all decrease by the same factor (κ). So how is it that smaller transistors with less current are able to produce faster circuits? The speed of a transistor circuit is determined by the rate at which a logic element (such as an inverter) can change from one state to another. This switching requires the charging or discharging of a capacitor at the output node (i.e., another device in the circuit). Because capacitance $C = (W_{ch} \cdot L_{ch} \cdot \varepsilon\varepsilon_o)/t_{ox}$, the total gate capacitance will decrease by the scaling factor κ. The charge required to charge a capacitor is Q = CV, which

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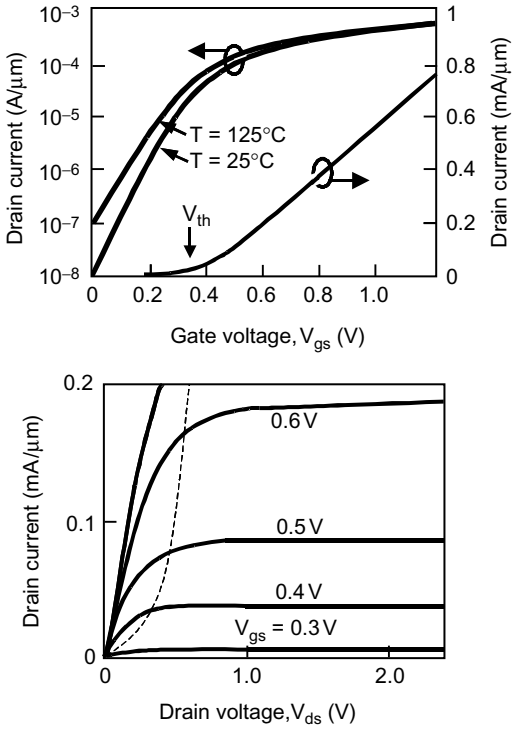

FIGURE 3.4 Operating characteristics for a typical MOS device. (a) Current measured at the drain as a function of voltage applied to the gate. The same data is plotted on linear and logarithmic scales. An extrapolation of the linear data is an estimate of the threshold voltage V_{th}. The slope of the data on the logarithmic scale for $V < V_{th}$ gives the subthreshold slope. Note that the device remains operational at temperatures >100°C, with an increase in inverse subthreshold slope and an increase in off-current (I_{off}) as temperature is increased. (b) Current measured at the drain as a function of source/drain voltage for various values of gate voltage for the same device as in (a). The dashed line indicates the transition to current saturation.

means that a reduction in C and a reduction in V by the factor κ results in a decrease in the total charge required by a factor of κ^2. Therefore, the decrease in current by κ still results in an increase in charging rate by the scaling factor κ, enabling the circuit speed to increase by a similar factor.

Another way to think about this is to directly calculate the time that it takes to charge the circuit output node. The charging rate of a capacitor is:

$$\frac{\partial V}{\partial t} = \frac{\boldsymbol{I}}{C} \tag{3.3}$$

where C is the total capacitance in Farads. Because I and C both decrease with size, the charging rate is also independent of size. However, because the smaller device will operate at a smaller voltage, then the time that it takes to charge will decrease (and the circuit will become faster) as size decreases. An expression for charging time is obtained by integrating Equation 3.3, where $V = V_{sd}$, $I = I_{sd}$, and $C = (C_{ox} \cdot L_{ch} \cdot W_{ch})$; and substituting in for current from the mobility expression (Equation 3.1):

$$t = \frac{L_{ch}^2}{\mu_{eff}(V_{gs} - V_{th})} \tag{3.4}$$

This shows that as V_{gs} and L_{ch} decrease by κ, the charging time will also decrease by the same factor, leading to an increase in circuit speed.

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3.3.2 Constant Field Scaling and Power Dissipation

As discussed in the SIA Roadmap, significant attention is currently paid to issues in front-end silicon processing. One of the most demanding challenges is new dielectric materials to replace silicon dioxide to achieve high gate capacitance with low gate leakage.[14] The need for higher capacitance with low leakage is driven primarily by the need for improved device speed while maintaining low power operation. Power has been an overriding challenge in MOS technologies since the early days of electronics, long before the relatively recent interest in portable systems. For example, reduced power consumption was one of the important problems that drove replacement of vacuum tubes with solid-state electronics in the 1950s and 1960s. Low power is required primarily to control heat dissipation, since device heating can significantly reduce device performance (especially if the device gets hot enough to melt). For current technology devices, dissipation of several watts of heat from a logic chip can be achieved using air cooling; and inexpensive polymer-based packaging approaches can be used. The increase in portable electronics has further increased the focus on problems associated with low power operation.

There are several possible approaches to consider when scaling electronic devices, including constant field and constant voltage scaling. Because of the critical need for low heat generation and power dissipation, current trends in shrinking CMOS transistor design are based on the rules of constant field scaling. Constant field scaling is an idealized set of scaling rules devised to enable device dimensions to decrease while output power density remains fixed. As discussed briefly above, constant field scaling cannot be precisely achieved, primarily because of nonscaling of the voltage threshold. Therefore, modifications in the ideal constant field scaling rules are made as needed to optimize device performance. Even so, the trends of constant field scaling give important insight into engineering challenges facing any advanced electronic device (including molecular circuits); therefore, the rules of constant field scaling are discussed here.

Heat generation in a circuit is related to the product of current and voltage. In a circuit operating at frequency f, the current needed to charge a capacitor C_T in half a cycle time is $(f \cdot C_T \cdot V_{dd})/2$, where V_{dd} is the applied voltage. Therefore, the power dissipated in one full cycle of a CMOS switching event (the *dynamic power*) is proportional to the total capacitance that must be charged or discharged during the switching cycle, C_T (i.e., the capacitance of the output node of the logic gate), the power supply voltage squared, V_{dd}^2, and the operation frequency, f:

$$\boldsymbol{P_{switch}} = fC_T V_{dd}^2 \tag{3.5}$$

The capacitance of the output node is typically an input node of another logic gate (i.e., the gate of another CMOS transistor). If a chip has ~10^8 transistors/cm^2, a gate length of ~130 nm, and width/length ratio of 3:1, then the total gate area is ~ 5% of the chip area. Therefore, the total power consumed by a chip is related to the capacitance density of an individual transistor gate ($C/A = \varepsilon\varepsilon_o/t_{ox}$).

$$\begin{aligned} \frac{P_{switch}}{A_{gate}} &= \frac{f\varepsilon\varepsilon_O V_{dd}^2}{t_{ox}} \\ \frac{P_{chip}}{A_{chip}} &\approx 0.05\left(\frac{P_{switch}}{A_{gate}}\right) \end{aligned} \tag{3.6}$$

where t_{ox} is the thickness and ε is the dielectric constant of the gate insulator. This is a highly simplified analysis (a more complete discussion is given in Reference 15). It does not include the power loss associated with charging and discharging the interconnect capacitances, and it does not include the fact that in CMOS circuits, both NMOS and PMOS transistors are partially on for a short time during the switching transition, resulting in a small current flow directly to ground, contributing to additional power loss. It also assumes that there is no leakage through the gate dielectric and that current flow in the off state is negligible. Gate leakage becomes a serious concern as dielectric thickness decreases and tunneling increases, and off-state leakage becomes more serious as the threshold voltage decreases. These two processes result in an additional *standby power* term ($P_{standby} = I_{off} \cdot V_{dd}$) that must be added to the power loss analysis.

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Even with these simplifications, the above equation can be used to give a rough estimate of power consumption by a CMOS chip. For example, for a 1GHz chip with V_{dd} of ~1.5V and gate dielectric thickness of 2 nm, the above equation results in ~150 W/cm^2, which is within a factor 3 of the ~50W/cm^2 dissipated for a 1GHz chip.[16] The calculation assumes that all the devices are switching on each cycle. Usually, only a fraction of the devices will switch per cycle, and the chip will operate with maximum output for only short periods, so the total power output will be less than the value calculated. A more complete calculation must also consider additional capacitances related to fan-out and loading of interconnect transmission lines, which will lead to power dissipation in addition to that calculated above. It is clear that heat dissipation problems in high-density devices are significant, and most high-performance processors require forced convection cooling to maintain operating temperatures within the maximum operation range of 70–80°C.[16]

The above relation for power consumption (Equation 3.5) indicates that in order to maintain power density, increasing frequency requires a scaled reduction in supply voltage. The drive to reduce V_{dd} in turn leads to significant challenges in channel and contact engineering. For example, the oxide thickness must decrease to maintain sufficient charge density in the channel region, but it must not allow significant gate leakage (hence the drive toward high dielectric constant insulators). Probably the most challenging problem in V_{dd} reduction is engineering of the device threshold voltage, V_{th}, which is the voltage at which the carrier velocity approaches saturation and the device turns on. If V_{th} is too small, then there is significant off-state leakage; and if it is too close to V_{dd}, then circuit delay becomes more problematic.

The primary strength of silicon device engineering over the past 20 years has been its ability to meet the challenges of power dissipation, enabling significant increases in device density and speed while controlling the temperature increases associated with packing more devices into a smaller area. To realize viable molecular electronic devices and systems, technologies for low-power device operation and techniques that enable power-conscious scaling methodologies must be developed. Discussion of power dissipation in molecular devices — and estimations of power dissipation in molecular circuits in comparison with silicon — have not been widely discussed, but are presented in detail below.

The steady-state operating temperature at the surface of a chip can be roughly estimated from Fourier's law of heat conduction:

$$Q = U\,\Delta T \tag{3.7}$$

where Q is the power dissipation per unit area, U is the overall heat transfer coefficient, and ΔT is the expected temperature rise in the system. The heat generated per unit area of the chip is usually transferred by conduction to a larger area where it is dissipated by convection. If a chip is generating a net ~100mW/cm^2 and cooling is achieved by natural convection (i.e., no fan), then U~20W/(m^{2}K),[17] and a temperature rise of 50°C can be expected at the chip surface. (Many high-performance laptops are now issued with warnings regarding possible burns from contacting the hot casing surface.) A fan will increase U to 50W/(m^{2}K) or higher. Because constant field scaling cannot be precisely achieved in CMOS, the power dissipation in silicon chips is expected to increase as speed increases; and there is significant effort under way to address challenges specific to heat generation and dissipation in silicon device engineering. Organic materials will be much more sensitive to temperature than current inorganic electronics, so *the ability to control power consumption and heat generation will be one of the overriding challenges that must be addressed to achieve viable high-density and high-speed molecular electronic systems.*

3.3.3 Interconnects and Parasitics

For a given supply voltage, the signal delay in a CMOS circuit is determined by the charge mobility in the channel and the capacitance of the switch. Several other *parasitic* resistance and capacitance elements can act to impede signal transfer in the circuit. The delay time of a signal moving through a circuit (τ) is given by the product of the circuit resistance and capacitance: $\tau = RC$, and parasitic elements add resistance and capacitance on top of the intrinsic R and C in the circuit. Several parasitic resistances and capacitances exist within the MOS structure itself, including contact resistance, source/drain and "spreading" resistance, gate/source overlap capacitance, and several others.

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Also important are the resistance and capacitance associated with the lines that connect one circuit to another. These interconnects can be local (between devices located close to each other on the chip) or global (between elements across the length of the chip). As devices shrink, there are significant challenges in interconnect scaling. Local interconnects generally scale by decreasing wire thickness and decreasing (by the same factor) the distance between the wires. When the wires are close enough that the capacitance between neighboring wires is important (as it is in most devices), the total capacitance per unit length C_L does not depend on the scaling factor. Because the resistance per unit length R_L increases as the wire diameter squared and the wire length decreases by L, then the delay time $\tau \sim R_L C_L L^2$ is not changed by device scaling. Moreover, using typical materials (Cu and lower-k dielectrics) in current device generations, local interconnect RC delay times do not significantly affect device speed. In this way, local interconnect signal transfer rates benefit from the decreasing length of the local interconnect lines. Global interconnects, on the other hand, generally increase in length as devices shrink due to increasing chip sizes and larger numbers of circuits per chip. This leads to significant signal delay issues across the chip. Solving this problem requires advanced circuit designs to minimize long interconnects and to reduce R_L and C_L by advanced materials such as high-conductivity metals and low dielectric constant insulators. This also implies that if sufficient function could be built into very small chips (much less than a few centimeters), using molecular components for example, issues of signal delay in global interconnects could become less of a critical issue in chip operation. However, sufficient current is needed in any network structure to charge the interconnecting transfer line. If designs for molecular devices focus on low current operation, then there may not be sufficient currents to charge the interconnect in the cycle times needed for ultrafast operation.

In addition to circuit performance, another concern for parasitic resistance and capacitance is in structures developed for advanced device testing. This will be particularly important as new test structures are developed that can characterize small numbers of molecules. As device elements decrease in size, intrinsic capacitances will increase. If the test structure contains any small parasitic capacitance in series or large parasitic capacitance in parallel with the device under test, the parasitic can dominate the signal measured. Moreover, in addition to difficulties associated with small current measurements, there are some significant problems associated with measuring large-capacitance devices (including ultrathin dielectric films), where substantial signal coupling between the device and the lead wires, for example, can give rise to spurious parasitic-related results.

3.3.4 Reliability

A hallmark attribute of solid-state device technology recognized in the 1940s was that of reliability. Personal computer crashes may be common (mostly due to software problems), but seldom does a PC processor chip fail before it is upgraded. Mainframe systems, widely used in finance, business, and government applications, have reliability requirements that are much more demanding than PCs; and current silicon technology is engineered to meet those demands. One of the most important modes of failure in CMOS devices is gate dielectric breakdown.[14] Detailed mechanisms associated with dielectric breakdown are still debated and heavily studied, but most researchers agree that charge transport through the oxide, which occurs in very small amounts during operation, helps create defects which eventually create a shorting path (breakdown) across the oxide. Defect generation is also enhanced by other factors, such as high operation temperature, which links reliability to the problem of power dissipation. Working with these restrictions, silicon devices are engineered to minimize oxide defect generation; and systems with reliable operation times exceeding 10 years can routinely be manufactured.

3.3.5 Alternate Device Structures for CMOS

It is widely recognized that CMOS device fabrication in the sub-50 nm regime will put significant pressure on current device designs and fabrication approaches. Several designs for advanced structures have been proposed, and some have promising capabilities and potential to be manufacturable.[18–22] Some of these structures include dual-gate designs, where gate electrodes on top and bottom of the

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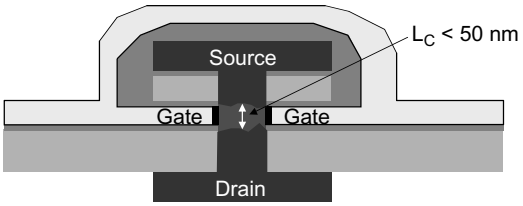

FIGURE 3.5 Schematic diagram of an example vertical field-effect transistor. For this device, the current between the source and drain flows in the vertical direction. The channel material is formed by epitaxial growth, where the channel length (L_c) is controlled by the film thickness rather than by lithography.

channel (or surrounding the channel) can increase the current flow by a factor of 2 and reduce the charging time by a similar factor, as compared with the typical single-gate structure. Such devices can be partially depleted or fully depleted, depending on the thickness of the channel layer, applied field, and dielectric thickness used. Many of these devices rely on silicon-on-insulator (SOI) technology, where very thin crystalline silicon layers are formed or transferred onto electrically insulating amorphous dielectric layers. This electrical isolation further reduces capacitance losses in the device, improving device speed.

Another class of devices gaining interest is vertical structures. A schematic of a vertical device is shown in Figure 3.5. In these devices, the source and drain are on top and bottom of the channel region; and the thickness of the channel region is determined relatively easily by controlling the thickness of a deposited layer rather than by lithography. Newly developed thin film deposition approaches, such as atomic layer deposition, capable of highly conformal coverage of high dielectric constant insulators, make these devices more feasible for manufacturing with channel length well below 50 nm.[19]

3.4 Memory Devices

3.4.1 DRAM, SRAM, and Flash

The relative simplicity of memory devices, where in principle only two contact terminals are needed to produce a memory cell, makes memory an attractive possible application for molecular electronic devices. Current computer random access memory (RAM) is composed of dynamic RAM (DRAM), static RAM (SRAM), and flash memory devices. SRAM, involving up to six transistors configured as cross-coupled inverters, can be accessed very quickly; but it is expensive because it takes up significant space on the chip. SRAM is typically small (~1MB) and is used primarily in processors as cache memory. DRAM uses a storage capacitor and one or two transistors, making it more compact than SRAM and less costly to produce. DRAM requires repeated refreshing, so cycle times for data access are typically slower than with SRAM. SRAM and DRAM both operate at typical supply voltage, and the issue of power consumption and heat dissipation with increased memory density is important, following a trend similar to that for processors given in Equations 3.5 and 3.6. Overall power consumption per cm^2 for DRAM is smaller than that for processors. Flash memory requires higher voltage, and write times are slower than for DRAM; but it has the advantage of being nonvolatile. Power consumption is important for flash since it is widely used in portable devices.

3.4.2 Passive and Active Matrix Addressing

It is important to note that even though DRAM operates by storing charge in a two-terminal capacitor, it utilizes a three-terminal transistor connected to each capacitor to address each memory cell. This *active matrix* approach can be contrasted with a *passive matrix* design, where each storage capacitor is addressed by a two-terminal diode. The passive addressing approach is much more simple to fabricate, but it suffers from two critical issues: cross-talk and power consumption. Cross-talk is associated with fringing fields, where the voltage applied across a cell results in a small field across neighboring cells; and this becomes

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more dominant at higher cell density. The fringing field is a problem in diode-addressed arrays because of the slope of the diode current vs. voltage (IV) curve and the statistical control of the diode turn-on voltage. Because the diode IV trace has a finite slope, a small voltage drop resulting from a fringing field will give rise to a small current that can charge or discharge neighboring cells. The diode-addressing scheme also results in a small voltage drop across all the cells in the row and column addressed. Across thousands of cells, this small current can result in significant chip heating and power dissipation problems.

An active addressing scheme helps solve problems of cross-talk and power dissipation by minimizing the current flow in and out of cells not addressed. The steep logarithmic threshold of a transistor (Equation 3.2) minimizes fringing field and leakage problems, allowing reliable operation at significantly higher densities. The importance of active addressing schemes is not limited to MOS memory systems. The importance of active matrix addressing for flat panel displays has been known for some time,[23] and active addressing has proven to be critical to achieve liquid crystal displays with resolution suitable for most applications. Well-controlled manufacturing has reduced costs associated with active addressing, and many low-cost products now utilize displays with active matrix addressing.

Molecular approaches for matrix-array memory devices are currently under study by several groups. Challenges addressed by silicon-based memory, including the value and statistical control of the threshold slope, will need to be addressed in these molecular systems. It is likely that, at the ultrahigh densities proposed for molecular cross-bar array systems, some form of active matrix addressing will be needed to control device heating. This points to the importance of three-terminal switching devices for molecular systems.

3.5 Opportunities and Challenges for Molecular Circuits

The above discussion included an overview of current CMOS technology and current directions in CMOS scaling. The primary challenges in CMOS for the next several generations include lithography and patterning, tolerance control, scaling of threshold and power supply voltages, controlling high-density dopant concentration and concentration profiles, improving contact resistance and capacitances, increasing gate capacitance while reducing gate dielectric tunneling leakage, and maintaining device performance (i.e., mobility and subthreshold slope). These issues can be summarized into (at least) six distinct engineering challenges for any advanced electronic system:

- Material patterning and tolerance control
- Reliability
- Interconnects and parasitics
- Charge transport (including device speed and the importance of contacts and interfaces)
- Power and heat dissipation
- Circuit and system design and integration (including use of gain)

These challenges are not unique to CMOS or silicon technology, but they will be significant in any approach for high-density, high-speed electronic device technology (including molecular electronics). For molecular systems, these challenges are in addition to the overriding fundamental material challenges associated with design and synthesis, charge transport mechanisms, control of electrostatic and contact potentials, etc.

It is possible that alternate approaches could be developed to circumvent some of these challenges. For example, high-density and highly parallel molecular computing architectures could be developed such that the speed of an individual molecular device may not need to follow the size/speed scaling rules. It is important to understand, however, that the engineering challenges presented above must be addressed together. An increase in parallelism may enable lower device speeds, but it puts additional demands on interconnect speed and density, with additional problems in parasitics, heat and power dissipation, contacts, etc.

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Lithography-based approaches to form CMOS device features less than 20 nm have been demonstrated[24,25] (but not perfected), and most of the other engineering challenges associated with production of 10–20 nm CMOS devices have yet to be solved. It is clear that Moore's law cannot continue to atomic-scale silicon transistors. This raises some natural questions:

1. At what size scale will alternate material technologies (such as quantum or molecular electronics) have a viable place in engineered electronic systems?
2. What fundamental material challenges should be addressed now to enable required engineering challenges to be met?

The theoretical and practical limits of silicon device speed and size have been addressed in several articles,[2–4,26–29] and results of these analyses will not be reviewed here. In this section, several prospective molecular computing architectures will be discussed in terms of the six engineering challenges described above. Then a prospective hybrid silicon/molecular electronics approach for engineering and implementing molecular electronic materials and systems will be presented and discussed.

3.5.1 Material Patterning and Tolerances

As devices shrink and numbers of transistor devices in a circuit increase, and variations occur in line width, film thickness, feature alignment, and overlay accuracy across a chip, significant uncertainty in device performance within a circuit may arise. This uncertainty must be anticipated and accounted for in circuit and system design, and significant effort focuses on statistical analysis and control of material and pattern tolerances in CMOS engineering. Problems in size and performance variations are expected to be more significant in CMOS as devices continue to shrink. Even so, alignment accuracy and tolerance currently achieved in silicon processing are astounding (accuracy of ~50 nm across 200 mm wafers, done routinely for thousands of wafers). The attraction of self-assembly approaches is in part related to prospects for improved alignment and arrangement of nanometer-scale objects across large areas. Nanometer scale arrangement has been demonstrated using self-assembly approaches, but reliable self-assembly at the scale approaching that routinely achieved in silicon manufacturing is still a significant challenge. Hopefully, future self-assembly approaches will offer capabilities for feature sizes below what lithography can produce at the time. What lithography will be able to achieve in the future is, of course, unknown.

3.5.2 Reliability

As discussed above, reliable operation is another hallmark of CMOS devices; and systems with reliable operation times exceeding 10 years can be routinely manufactured. Achieving this level of reliability in molecular systems is recognized as a critical issue, but it is not yet widely discussed. This is because molecular technology is not yet at the stage where details of various approaches can be compared in terms of reliability, and fundamental mechanisms in failure of molecular systems are not yet discernible. Even so, some general observations can be made. Defect creation energies in silicon-based inorganic materials are fairly well defined. Creating a positive charged state within the silicon band gap, for example, will require energies in excess of silicon's electron affinity (> 4.1 eV). Ionization energies for many organic electronic materials are near 4–5 eV, close to that for silicon; but deformation energies are expected to be smaller in the organics, possibly leading to higher energy defect structures where less excess energy is needed to create active electronic defects. Therefore, reliability issues are expected to be more problematic in molecular systems as compared with silicon. Other factors such as melting temperatures and heat capacity also favor inorganic materials for reliable and stable operation. *Defect tolerant* designs are being considered that could overcome some of the problems of reliably interconnecting large numbers of molecular scale elements.[30] However, it is not clear how, or if, such an approach would manage a system with a defect density and distribution that changes relatively rapidly over time.

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3.5.3 Interconnects, Contacts, and the Importance of Interfaces

Interconnection of molecular devices is also recognized as a critical problem. Fabrication and manipulation of molecular scale wires is an obvious concern. The size and precision for manipulating the wires must reach the same scale as the molecules. Otherwise, the largest device density would be determined by the density of the interconnect wire packing (which may not be better than future silicon devices) — not by the size of the molecules. Multilevel metallization technology is extremely well developed and crucial for fully integrated silicon systems; but as yet, no methodologies for multilevel interconnect have been demonstrated. Approaches such as metal nanocluster-modified viral particles[6] under study at the Naval Research Lab are being developed, in part, to address this issue. Also, as discussed above in relation to silicon technology, approaches will be needed to isolate molecular interconnections to avoid cross-talk and RC signal decay during transmission across and among chips. These problems with interconnect technology have the potential to severely limit realistic implementation of molecular-scale circuits.

The need to connect wires to individual molecules presents another set of problems. Several approaches to engineer linker elements within the molecular structure have been successful to achieve high-quality molecular monolayers on metals and other surfaces, and charge transport at molecule/metal surfaces is well established. However, the precise electronic structure of the molecule/metal contact and its role in the observed charge transport are not well known. As more complex material designs are developed to achieve molecular-scale arrays, other materials will likely be needed for molecular connections; and a more fundamental understanding of molecule/solid interfaces will be crucial. One specific concern is molecular conformational effects at contacts. Molecules can undergo a change in shape upon contact with a surface, resulting in a change in the atomic orbital configurations and change in the charge transfer characteristics at the interface. The relations among adsorption mechanisms, interface bond structure, configuration changes, and interface charge transfer need to be more clearly understood.

3.5.4 Power Dissipation and Gain

3.5.4.1 Two-Terminal Devices

The simplest device structures to utilize small numbers of molecules and to take advantage of self-assembly and "bottom-up" device construction involve linear molecules with contacts made to the ends. These can operate by quantum transport (i.e., conduction determined by tunneling into well-defined energy levels) or by coulomb blockade (i.e., conduction is achieved when potential is sufficient to overcome the energy of charge correlation). Molecular "shuttle" switches[31,32] are also interesting two-terminal structures. Two-terminal molecules can be considered for molecular memory[33–35] and for computation using, for example, massively parallel crossbar arrays[30] or nanocells.[36] All of the engineering challenges described above will need to be addressed for these structures to become practical, but the challenges of gain and power dissipation are particularly demanding.

The lack of gain is a primary problem for two-terminal devices, and signal propagation and fan-out must be supported by integration of other devices with gain capability. This is true for computation devices and for memory devices, where devices with gain will be needed to address and drive a memory array. Two-terminal logic devices will also suffer from problems of heat dissipation. The power dissipation described above in Equations 3.5 and 3.6 corresponds only to power lost in capacitive charging and discharging (dynamic power dissipation) and assumes that current does not flow under steady-state operation. The relation indicates that the dynamic power consumption will scale with the capacitance (i.e., the number of charges required to change the logic state of the device), which in principle could be small for molecular devices. However, quantum transport devices can have appreciable current flowing at steady state, adding another *standby power* term:

$$P_{standby} = I_{off} \cdot V_{dd} \tag{3.8}$$

where I_{off} is the integrated current flow through the chip per unit area during steady-state operation. As discussed in detail above, complementary MOS structures are widely used now primarily because they

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can be engineered to enable negligible standby current (I_{off}). Standby power will be a serious concern if molecular devices become viable, and approaches that enable complementary action will be very attractive.

The relations above show that operating voltage is another important concern. Most molecular devices demonstrated to date use fairly high voltages to produce a switching event, and the parameters that influence this threshold voltage are not well understood. Threshold parameters in molecular devices must be better understood and controlled in order to manage power dissipation. Following the heat transfer analysis in Equation 3.7, generation of only ~200 mW/cm^2 in a molecular system cooled by natural convection would likely be sufficient to melt the device!

3.5.4.2 Multiterminal Structures

There are several examples of proposed molecular-scale electronic devices that make use of three or more terminals to achieve logic or memory operation. Approaches include the single electron transistor (SET),[11] the nanocell,[36] quantum cellular automata (QCA),[37] crossed or gated nanowire devices,[38–41] and field-effect devices with molecular channel regions.[42,43] Of these, the SET, nanowire devices, and field-effect devices are, in principle, capable of producing gain.

The nanocell and QCA structures are composed of sets of individual elements designed and organized to perform as logic gates and do not have specific provisions for gain built into the structures. In their simplest operating forms, therefore, additional gain elements would need to be introduced between logic elements to maintain signal intensity through the circuit. Because the QCA acts by switching position of charge on quantum elements rather than by long-range charge motion, the QCA approach is considered attractive for low power consumption. However, power will still be consumed in the switching events, with a value determined by the dynamic power equation (Equation 3.6). This dynamic power can be made small by reducing the QCA unit size (i.e., decreasing capacitance). However, reducing current will also substantially affect the ability to drive the interconnects, leading to delays in signal input and output. Also, the switching voltage must be significantly larger than the thermal voltage at the operating temperature, which puts a lower limit on V_{dd} and dynamic power consumption for these devices. The same argument for dynamic power loss and interconnect charging will apply to the switching processes in the nanocell device. The nanocell will also have the problem of standby power loss as long as NDR molecules have significant off-state leakage (i.e., low output impedance and poor device isolation). Output currents in the high impedance state are typically 1 pA, with as much as 1000 pA in the low impedance state. If a nanocell 1 μm $\times$ 1 μm contains 10^4 molecules,[36] all in the off state (I_{off} = 1pA) with V_{dd} = 2V, then the power dissipation is expected to be ~1 W/cm^2 (presuming 50% of the chip area is covered by nanocells). This power would heat the chip and likely impair operation substantially (from Equation 3.7, ΔT would be much greater than 100°C under natural convection cooling). Stacking devices in three-dimensional structures could achieve higher densities, but it would make the heat dissipation problem substantially worse. Cooling of the center of a three-dimensional organic solid requires conductive heat transfer, which is likely significantly slower than cooling by convection from a two-dimensional surface. To address these problems, molecular electronic materials are needed with smaller operating voltage, improved off-state leakage, better on/off ratios, and sharper switching characteristics to enable structures with lower load resistances. It is important to note one aspect of the nanocell design: it may eventually enable incorporation of pairs of RTD elements in "Goto pairs," which under a limited range of conditions can show elements of current or voltage gain.[36,44]

Some devices, including the single-electron transistor (SET),[45,46] crossed and gated nanowire devices,[38–41] and field-effect devices with molecular channel regions[42,43] show promise for gain at the molecular scale; but none has yet shown true molecular-scale room temperature operation. The nanowire approach is attractive because of the possible capability for complementary operation (i.e., possibly eliminating standby power consumption). Field-effect devices with molecular channel regions show intriguing results,[42,43] but it is not clear how a small voltage applied at a large distance (30 nm) can affect transport across a small molecule (2 nm) with a larger applied perpendicular field. Even so, approaches such as these, and others with the prospect of gain, continue to be critical for advanced development of fully engineered molecular-scale electronic devices and systems.

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3.5.5 Thin-Film Electronics

Thin-film electronics, based on amorphous silicon materials, is well established in device manufacturing. Charge transport rates in organic materials can challenge those in amorphous silicon; and organic materials may eventually offer advantages in simplicity of processing (including solution-based processing, for example), enabling very low-cost large-area electronic systems. The materials, fabrication, and systems engineering challenges for thin-film electronics are significantly different from those of potential single-molecule structures. Also, thin-film devices do not address the ultimate goal of high-density, high-speed electronic systems with molecular-scale individual elements. Therefore, thin-film electronics is typically treated as a separate topic altogether. However, some thin-film electronic applications could make use of additional functionality, including local computation or memory integrated within the large-area system. Such a system may require two distinctly different materials (for switching and memory, for example), and there may be some advantages of utilizing silicon and molecules together in hybrid thin-film inorganic/molecular/organic systems.

3.5.6 Hybrid Silicon/Molecular Electronics

As presented above, silicon CMOS technology is attractive, in large part, because of its ability to scale to very high densities and high speed while maintaining low power generation. This is achieved by use of: (1) complementary device integration (to achieve minimal standby power) and (2) devices with capability of current and voltage gain (to maintain the integrity of a signal as it moves within the circuit). Molecular elements are attractive for their size and possible low-cost chemical routes to assembly. However, the discussion above highlights many of the challenges that must be faced before realistic all-molecular electronic systems can be achieved.

A likely route to future all-molecular circuits is through engineered hybrid silicon/molecular systems. Realizing such hybrid systems presents additional challenges that are generally not addressed in studies of all-molecular designs, such as semiconductor/molecule chemical and electrical coupling, semiconductor/organic processing integration, and novel device, circuit, and computational designs. However, these additional challenges of hybrid devices are likely more surmountable in the near term than those of all-molecule devices and could give rise to new structures that take advantage of the benefits of molecules and silicon technology. For example, molecular RTDs assembled onto silicon CMOS structures could enable devices with multiple logic states, so more complex computation could be performed within the achievable design rules of silicon devices. Also, molecular memory devices integrated with CMOS transistors could enable ultrahigh density and ultrafast memories close-coupled with silicon to challenge SRAM devices in cost and performance for cache applications in advanced computing. Coupling molecules with silicon could also impact the problem of molecular characterization. As discussed above, parasitic effects in device characterization are a serious concern; and approaches to intimately couple organic electronic elements with silicon devices would result in structures with well-characterized parasitics, leading to reliable performance analysis of individual and small ensembles of molecules — critically important for the advance of any molecular-based electronic technology.

3.6 Summary and Conclusions

Present-day silicon technology is a result of many years of tremendously successful materials, device, and systems engineering. Proposed future molecular-based devices could substantially advance computing technology, but the engineering of proposed molecular electronic systems will be no less challenging than what silicon has overcome to date. It is important to understand the reasons why silicon is so successful and to realize that silicon has and will continue to overcome many substantial "show-stoppers" to successful production. Most of the engineering issues described above can be reduced to challenges in materials and materials integration. For example: can molecular switches with sufficiently low operating voltage and operating current be realized to minimize heat dissipation problems? Or: can charge coupling and transport through interfaces be understood well enough to design improved electrical

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contacts to molecules to control parasitic losses? It is likely that an integrated approach, involving close-coupled studies of fundamental materials and engineered systems including hybrid molecular/silicon devices, will give rise to viable and useful molecular electronic elements with substantially improved accessibility, cost, and capability over current electronic systems.

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